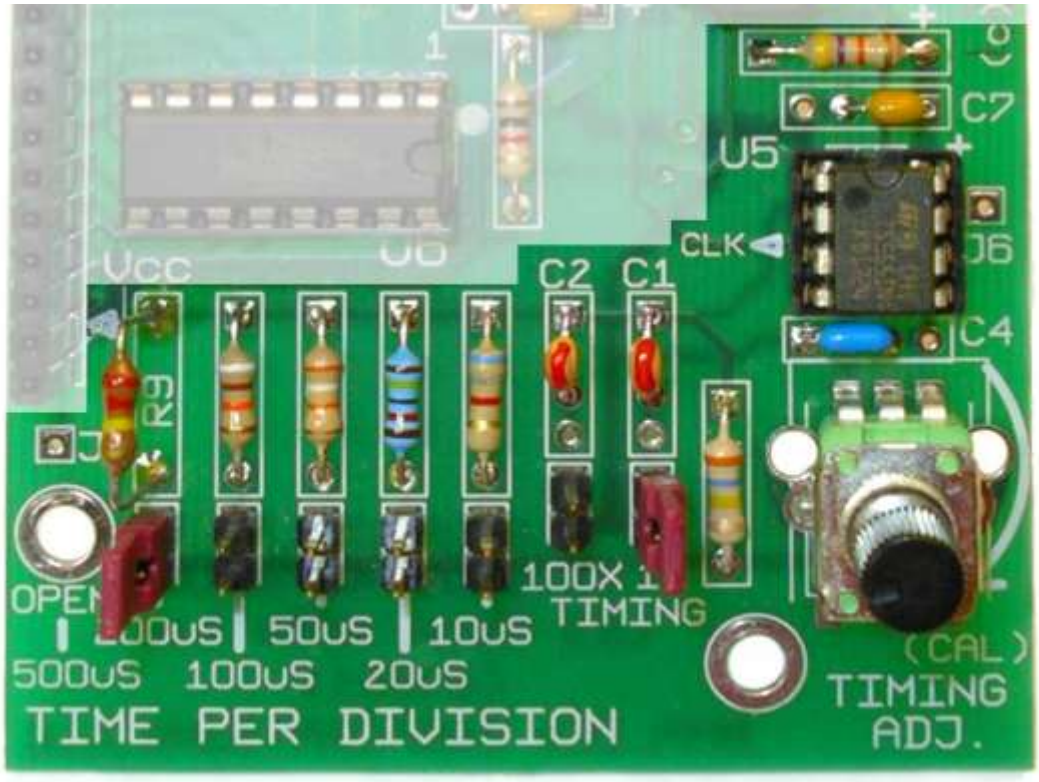
**L.E.D. Oscilloscope**
**L**earn **E**lectronics by **D**oing
- Theory is pretty thin stuff until it's mixed with experience.-

# Chapter 5
# System Timing




To be able to "sweep" the dot that represents voltage across our display, we need to select one column at a time along the X axis. To do this, we need something to set the timing between column selections. This is similar to the ticking of a clock, or a metronome when playing the piano. The circuit that generates the pulses used to set this timing is often referred to as "The System Clock" because these pulses are similar to the seconds of a clock's ticking, and because it is the master timing source. You have probably heard this term in reference to Personal Computers. The "clock speed" is the frequency of the pulses that determine how quickly the circuits switch from one condition to the next. For our oscilloscope, the clock circuit controls how quickly the X drive circuitry moves the dot across the display screen by selecting the next column for the Y driver to display. For the LED-Scope's system clock we will use a CMOS **TLC555** timer chip.

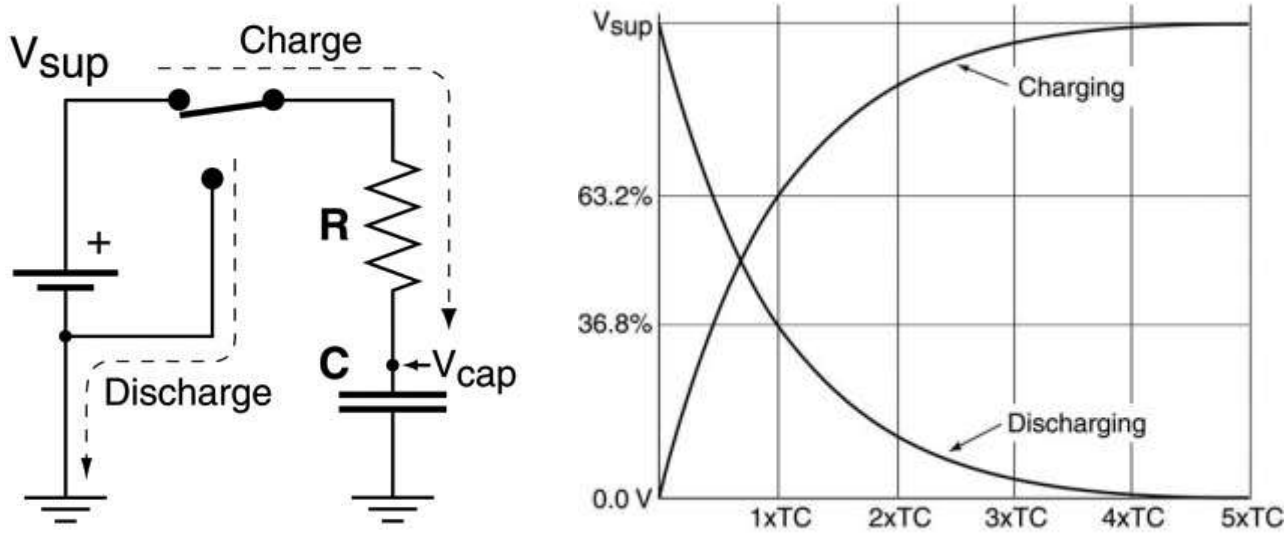
## The Versitile 555 Timer Chip

Signetics released the first 555 timer chip in 1971. Proof of its versatility is that it is still in production (40 years!), and about a 1 billion units are manufactured every year. It has been used in:

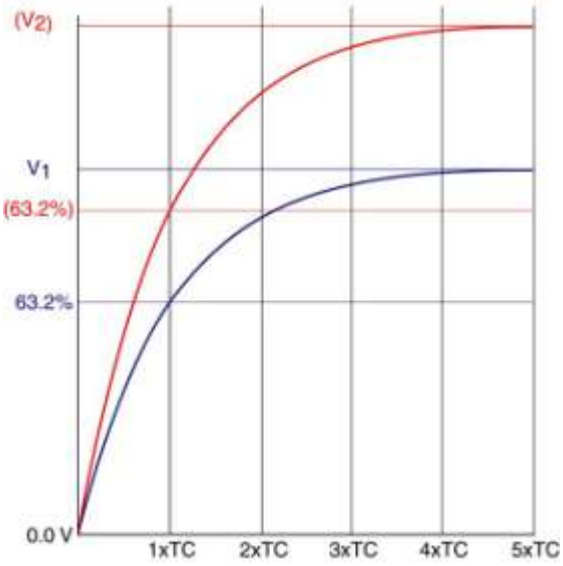
| | | |
|---|---|---|
| Sequential Timer | Rodent Repeller | Motor Speed Controllers |
| Tachometer | Time Delay Relay | Windshield Wiper Delay |
| Servo Controller | Blinker Controls | Voltage-to-Frequency Converters |
| Battery Chargers | Linear Ramp Generator | Sound Effect Generators |
| Lamp Dimmer | Alarm Systems | |
| Metronome | Audio Signal Generators | And it has even been used to build an AM radio! |

## Timing Elements

In chapter 11 of PArt-1, Basic Electronics, you charged and discharged a capacitor through a resistor. This is a basic Resistor-Capacitor or "RC" timing circuit. The term "RC time constant" refers to the length of time it will take for the capacitor, **C**, to charge up to 63.2% of the supply voltage through the resistor, **R**. It is also the length of time it takes for a fully charged capacitor to discharge down to 36.8% of the supply voltage. Note that the shape of the discharging curve is just the inverse (upside-down) version of the charging curve.




*A simple RC circuit with the switch in the Charge position and the graphs of $V_{cap}$ for charging and discharging compared to time.*

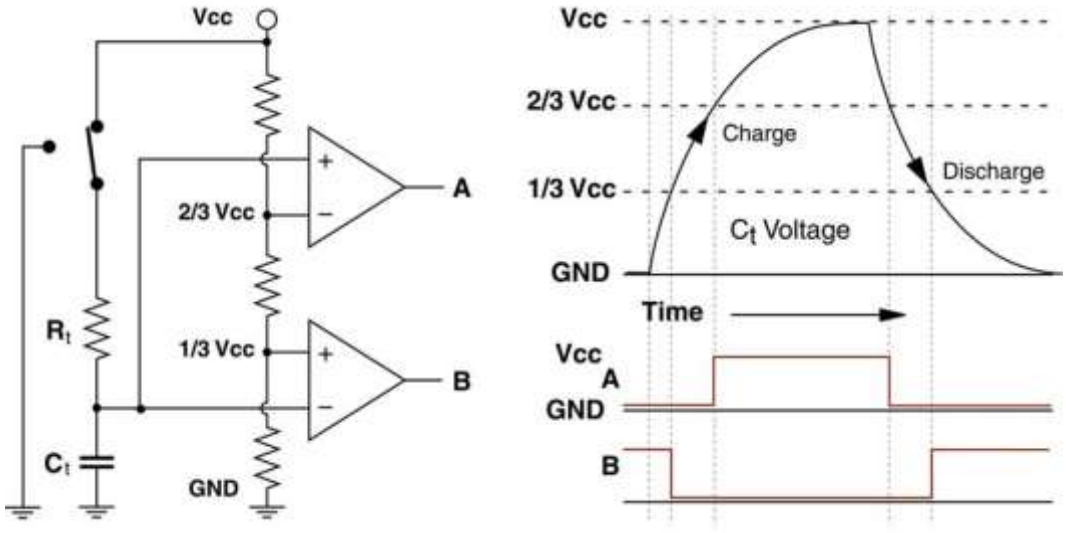



A special property of the RC time constant curve is that its shape does not change as the resistor, capacitor, or voltage values vary. This means that if we use an RC element in a timing circuit we can get very good stability and repeatability.

Note that one time constant (1xTC) for voltage 1 ($V_1$), is the same for voltage 2 ($V_2$).

## Analog to Digital

The charging and discharging voltage on the capacitor is a linear, analog value -- it varies smoothly between 0 and the supply voltage. Our clock signal needs to be digital -- in either an "On" or "Off" state. We can get a repeatable digital signal from our charge/discharge RC circuit by using the comparator element you learned about in chapter 3 and combining it with a voltage divider.




*This comparator configuration is sometimes called a "Window Comparator".*
*Both outputs will be low when the input voltage is in the "window" between 1/3 and 2/3 of Vcc.*

Now we have something closer to what we need. Note that the spacing between the "B" output turning off and the "A" turning on is consistent. Even if we increased or reduced Vcc, the time that they are both off will not change. Our problem now is that we need to get rid of the assistant who turns the switch on and off. We need a new circuit element that can be triggered by "A" and "B" to replace the switch.

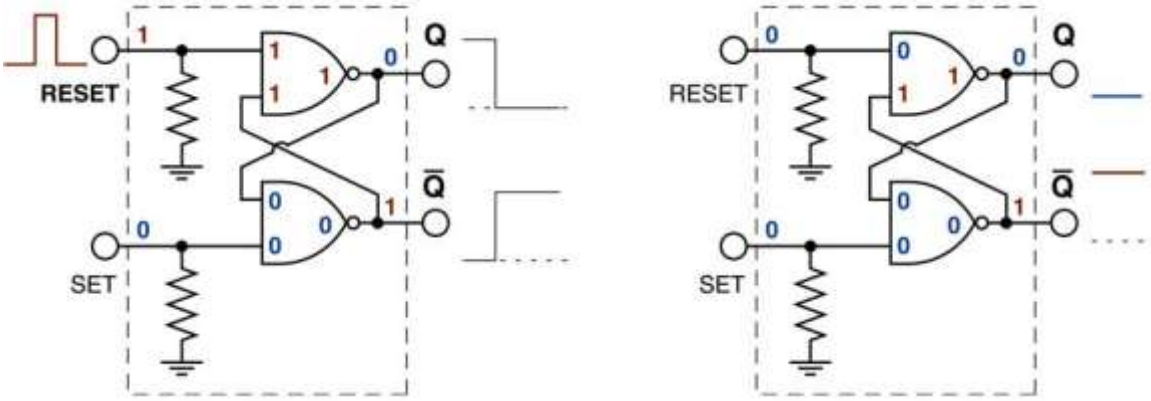
 

## Flip-Flop Memory Element

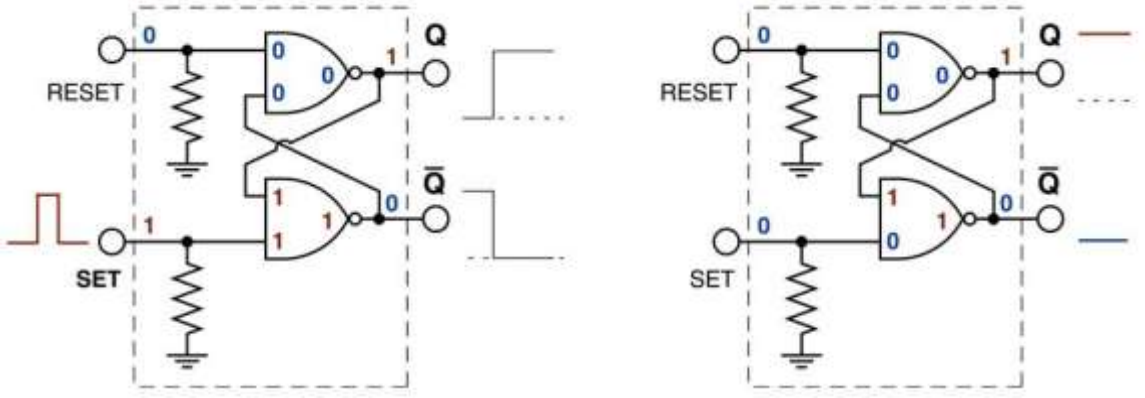
Now we need a circuit that can remember that event "B" occurred until "A" occurs, and then remember that event "A" occurred. In chapter 15 of Part-1, Basic Electronics, you tested something like this when you built the bi-stable flip-flop out of discrete transistors. A more responsive circuit can also be constructed from gates.

If we take 2 2-input NOR gates and cross connect them as shown in the following schematic, one will be forced to output a "1", and that will force the other to a "0". The circuit will stay latched in this state until a positive pulse on one of the inputs causes the state to change. Trace the signals through the schematic and follow the state changes.

**Review:** For an **OR** gate, a "1" on any input will make the output a "1", and the small circle inverts the logic (0 => 1 and 1=> 0), turning the **OR** gate in to a "**N**ot-**OR**" or **NOR** gate.



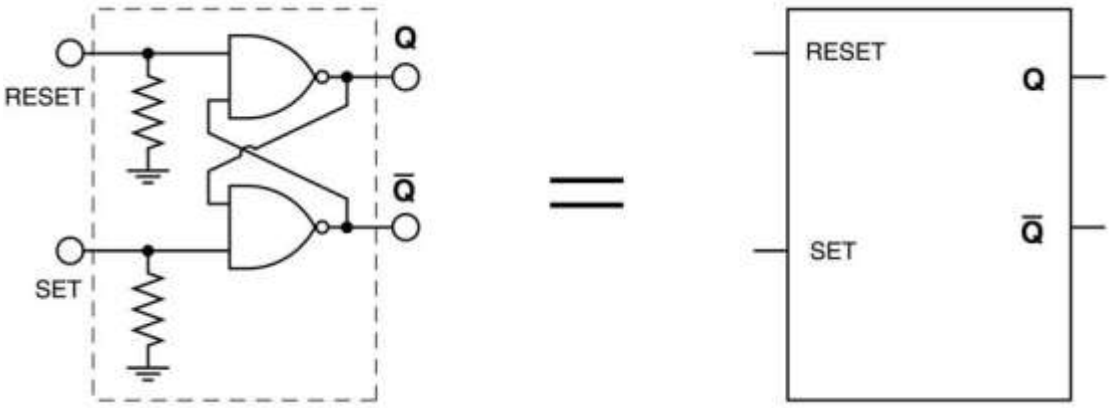

A positive pulse applied to the **RESET** line will force the output of the top NOR gate to go to "0". Because both inputs to the lower NOR gate are now "0", its output will be "1" and therefore maintain the output of the upper NOR gate at "0" even after the **RESET** line returns to "0".




A positive pulse applied to the **SET** line will cause a similar change of state: the output of the bottom NOR gate will go to "0", and both inputs to the upper NOR gate will now be "0", changing its output to "1" and therefore maintain the output of the lower NOR gate at "0".

We now have a circuit that will hold, or "latch" an input pulse.

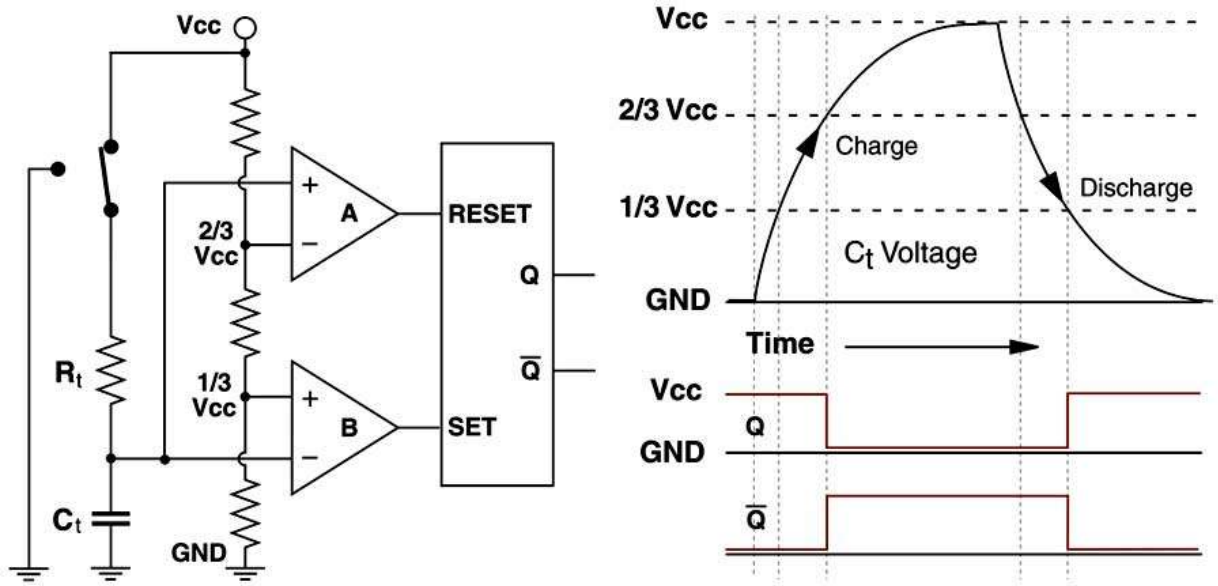
 




*Instead of drawing all the inner details, a simple function block can be used*

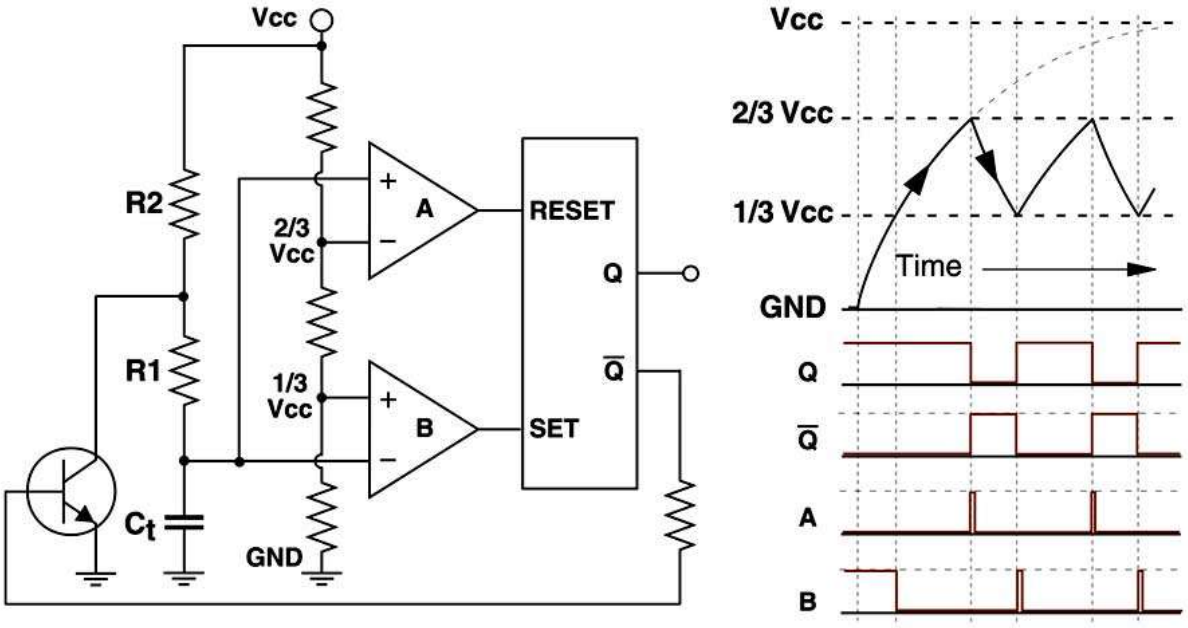
## Putting it All Together

Adding this to the RC and comparator circuit we already have will give us the next stage. Note that as soon as the voltage on the capacitor rises above the 2/3 Vcc point Q\ goes high.




If we send this signal to the base of a transistor, we can replace the SPDT (Single Pole Double Throw -- remember?) and use it instead to discharge the capacitor. Connecting the transistor's collector directly to the capacitor will instantly discharge it to ground, but this would be too fast and uncontrolled, so it is not a good choice. Connecting the transistor's collector above the timing resistor will now give the same discharge time as the charge time. But now we have a new problem -- we've just shorted the power supply to ground, so this will not work, though we are getting closer. The problem can be fixed by adding another resistor between the transistor connection and the power supply.




*We now have a stable, controllable oscillator. Note how the "A" and "B" Comparators only need to provide a tiny pulse to set or rest the flip-flop.*

With the basic design worked out, let's follow the circuit's operation, step by step, from when power is first applied.

**Let the fight begin . . .**

Initially all points in the circuit are at ground. When power is applied, the flip-flop outputs will start to "fight" for an initial state, since only one of them can be high at one time. But before they finish, the comparator will become active. Since the capacitor $C_t$ is discharged and at zero volts, the "A" comparator has zero volts on its "+" input and 2/3 of the supply voltage on the "-" input. For a comparator, the "-" being greater than the "+" means its output will be low -- at ground. The "B" comparator will have the opposite situation: zero volts on the "-" input and 1/3 supply voltage on the "+" input. This will cause its output to go high and ending the flip-flop battle. The Q output will now be high and the Q\ output will be Low.

**Round two:**

With no voltage supplied to the transistor's base, capacitor $C_t$ can start to charge through R1 and R2. As it does, it will reach a point where its voltage is above 1/3 supply voltage and the Set input to the flip-flop will go low, and the flip-flop will maintain its latched output. $C_t$'s voltage continues to climb until it reaches 2/3 of the supply voltage. Now the "A" comparator's output will go high and flip the state of the flip-flop so that Q is now low and Q\ is high.

**Round three:**

Q\ now applies voltage to the transistor's base, causing it to pass current from the collector to the emitter. This will "steal" the current available from R2 to charge $C_t$ and at the same time discharge capacitor $C_t$ through R1. As soon as $C_t$'s voltage drops just a little bit below 2/3 of the supply voltage, "A"s output will go back to zero, but the blow has been struck -- Q\ is still high and the transistor is still discharging the timing capacitor.

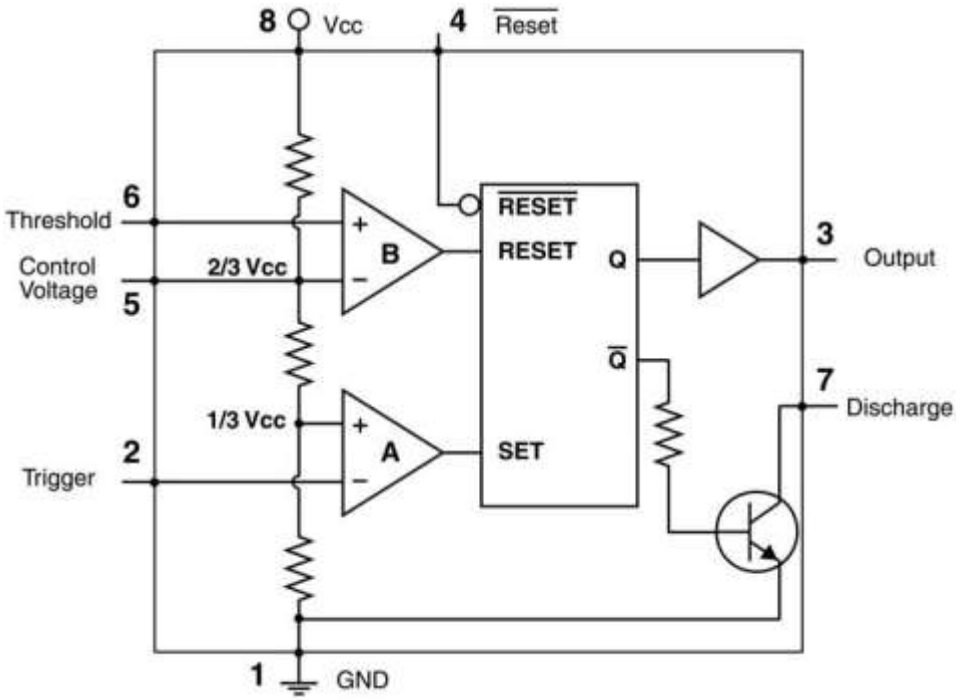
**Round Four:**
As $C_t$'s voltage continues to drop it will fall below 1/3 supply voltage and comparator "B" will spring into action and set Q high and Q\ to ground. With no voltage supply to the transistor's base, R2 will now supply current through R1 to recharge $C_t$ and its voltage will start to rise again. [I'm doing the best blow-by-blow narration I can here, but you really need to be following this on the schematic and timing graph.] When the voltage rises just a bit above 1/3 supply, the "B" comparator's output will go low, but the flip-flop will remember its current state and the transistor will remain off.

**Round Five, and around and around . . .**
$C_t$'s voltage will continue to climb up to 2/3 of the supply voltage, and the "A" comparator's output will go high and flip the state of the flip-flop once again, so that Q is now low and Q\ is high. We;ve seen this before in round three -- the transistor will discharge $C_t$, the comparators will do their jobs and flip the flip-flop, and the cycle will continue until power is removed.

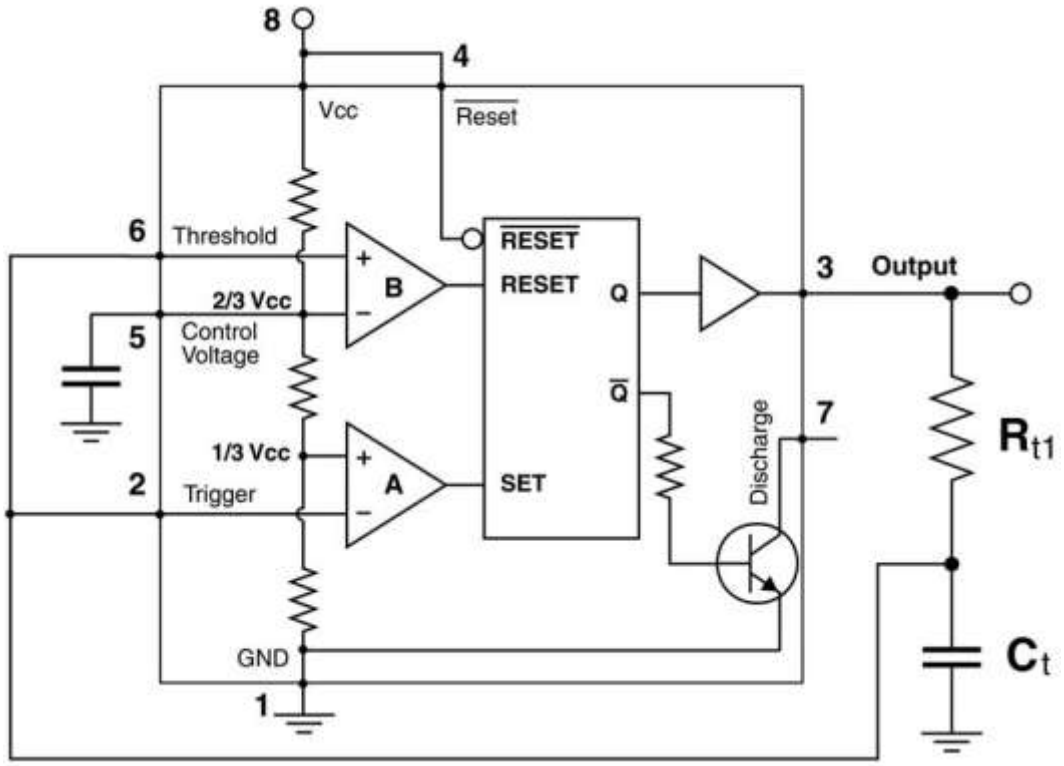
**A few fine points:**
Note that because the reference voltages supplied to the comparators are proportional to the supply voltage, variations in supply voltage will not affect the timing. The operating frequency will depend only on the values of R1, R2 and $C_t$. Also note that there is a larger total resistance value for the charging path than there is for the discharging path. This will result in an unsymmetrical square wave. Typically this is not a problem for circuits that will use this for their "clock" because they will typically use only the rising edge. If we need a symmetrical wave, we can come close by making R1 much bigger than R2. But, the smaller the value for R2, the greater the current through the transistor and our circuit will draw more power. If we just want very short, negative going pulses, things will be much more efficient.

The 555 timer chip adds a few extra features to increase this circuit's versatility. The output is buffered to provide more power to drive other circuits, and there is an external reset line available. This can be used by other circuit to turn the timer on and off. Finally, there is a tap provided to the resistor voltage divider network to allow linear control of the pulse widths by adjusting this voltage point from an outside source.




*The 555 Timer's internal functional blocks. This matches the circuit just developed with the addition of three more helpful features: a control voltage tap, a separate reset line, and an output buffer.*




*A CMOS 555 timer chip configured as a symmetrical square wave oscillator. The better output buffer drives both the RC and external circuitry. Only a single timing resistor is required.*

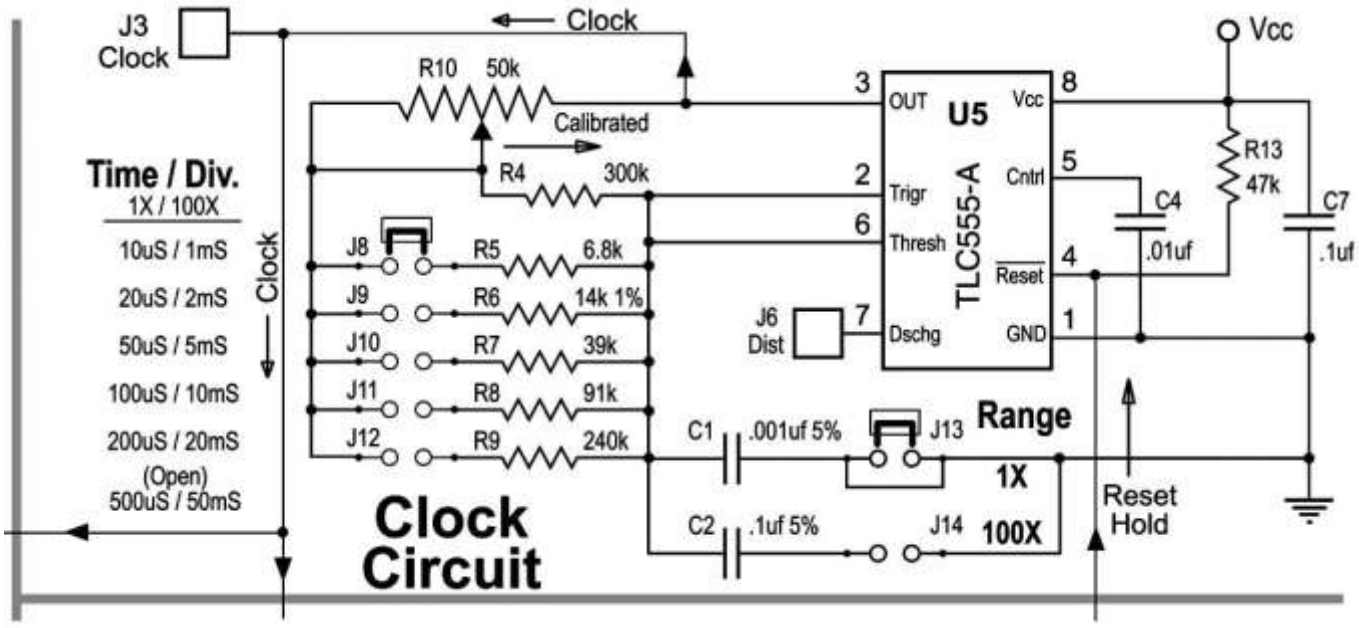
## 555 Timer Types

Because the original 555 timer chip was implemented in TTL (Transistor-Transistor-Logic) construction, it consumed a lot of current, typically 5-10ma, and its internal construction caused it to momentarily draw large currents when the output changed state. The application notes for the chip insisted that a large filter capacitor be placed across its ground and supply pins to prevent these current spikes from upsetting other ICs in a circuit. Newer versions have been implemented in CMOS technology, meaning they consume very little power (.065ma) and the output can swing fully from 0 to +5 volts. (Assuming a +5volt supply.) One of the biggest problems with the original TTL version was that the switching of the internal circuitry would momentarily draw a lot of current and cause power spikes that could disrupt other circuits.

## The System Clock Section - Part 1 of X-Drive Board

You will need the usual:
Safe work area

- Safety Glasses
- Power Supply module and Wall-Mount power module
- Piezo Speaker from Part 1
- Test leads from Chapter 2
- Tweezers, Pliers, Wire Cutters
- Soldering Iron & Stand or Soldering Station
- 63/37 Solder (or 60/40)
- Digital Multi Meter (DMM)
- X-Drive Parts Set




*System Clock Section using CMOS 555 Timer chip*

## Assembly

Setup your soldering station or iron as before, and let it come up to operating temperature.
The parts for this section are in the X-Drive Parts set:

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*[The assembly and testing sections follows the same sequence as in Part-1]*

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## Summary

- An RC time constant does not change when compared to a voltage proportional to the charging supply voltage. This can be used to provide good timing stability and repeatability.

- A "window comparator" consists of two comparators with the "+" input of one and the "-" of the other connected to a common signal source. Their alternate inputs are connected to separate voltage references that define the voltage "window".

- A Set-Rest Flip-Flop can be used as a memory element to hold the logic state of a previous condition so it can be compared to a later one.

- The 555 timer chip is composed of a "window comparator", supply voltage divider network, and a set-rest flip-flop. It is designed to be configured for timing application using a simple RC network. One of the most common is as an astable system clock oscillator.

- The newer CMOS (**C**omplementary **M**etal **O**xide **S**emiconductor) 555 timer chip provides even more versatility because of its high impedance inputs (read that as a large resistance or "they draw very, very, very, little current from other circuits"), and high current outputs while consuming very little power. (Something like 0.001 watts; A night light is 2 to 4 watts.)

- Without an oscilloscope (a condition soon to be remedied), we can use our ears to check to see if a clock circuit is oscillating by connecting a piezo speaker to the circuit.

- A piezo speaker can be used for quick tests because of its high impedance. This allows it to be connected to most circuits without causing problems because it is a small value capacitor.

- A regular loud speaker has a very low impedance and cannot be used like the piezo speaker.

- If the DMM has a frequency counter function, this can be used to measure the actual system clock frequency.

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